

**EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Glenn Barnes (Reg. No. 42,293) on 10/27/09.

The claims in the application have been amended as follows:

1. (Currently amended) A method comprising:  
executing virtual machine application instructions of a virtual machine application by using micro architecture code of a processor architecture;  
receiving an I/O access from the virtual machine application at a monitor supporting the virtual machine application;  
in response to receiving the I/O access, generating an exception;  
performing the I/O access by using a host operating system configured to support the monitor;  
updating state data for the virtual machine application at the monitor in accordance with the I/O access, the updating performed by a virtual machine component of the micro architecture code; and

resuming execution of the virtual machine application from the exception; and -  
wherein the micro architecture code comprises an instruction interpreter that functions  
with an instruction translator to execute the virtual machine application instructions, wherein the  
virtual machine application instructions comprise target instructions and the micro architecture  
code comprises host instructions.

8. (Cancelled)

9. (Currently amended) The method of claim 8\_1, wherein the target instructions  
comprise x86 instructions, and the host instructions comprise VLIW instructions.

10. (Currently amended) The method of claim 8\_1, wherein the virtual machine  
comprises an x86 compatible virtual machine.

11. (Currently amended) A system comprising:  
a processor architecture including micro architecture code that executes natively on a  
CPU hardware unit of the processor architecture; and  
a memory coupled to the processor architecture, the memory configured to store virtual  
machine application instructions of a virtual machine application, wherein the virtual machine  
application instructions are for execution using the micro architecture code to cause the system to  
implement a method comprising:

receiving an I/O access from the virtual machine application at a monitor supporting the virtual machine application;

in response to receiving the I/O access, generating an exception;

performing the I/O access by using a host operating system configured to execute on the processor architecture and to support the monitor; ~~and~~

updating state data for the virtual machine application at the monitor in accordance with the I/O access, the updating performed by a virtual machine component of the micro architecture code; ~~and~~

resuming execution of the virtual machine application from the exception; ~~and~~ .

wherein the micro architecture code comprises an instruction interpreter that functions with an instruction translator to execute the virtual machine application instructions, wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions.

18. (Cancelled)

19. (Currently amended) The system of claim ~~48~~ 11, wherein the target instructions comprise x86 instructions, and the host instructions comprise VLIW instructions.

20. (Currently amended) The system of claim ~~48~~ 11, wherein the virtual machine comprises an x86 compatible virtual machine.

21. (Currently amended) A computer readable medium having stored thereon, computer executable instructions that, if executed by a processor cause the processor to perform a method comprising:

executing virtual machine application instructions of a virtual machine application by using micro architecture code of a processor architecture;

receiving an I/O access from the virtual machine application at a monitor supporting the virtual machine application;

upon receiving the I/O access, generating an exception;

performing the I/O access by using a host operating system that executes on the processor architecture and that supports the monitor;

updating state data for the virtual machine application at the monitor in accordance with the I/O access, the updating performed by a virtual machine component of the micro architecture code; ~~and~~

resuming execution of the virtual machine application from the exception; ~~and~~ -

wherein the micro architecture code comprises an instruction interpreter that functions with an instruction translator to execute the virtual machine application instructions, wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions.

28. (Cancelled)

29. (Currently amended) The computer readable storage media of claim 28 21,  
wherein the target instructions comprise x86 instructions, and the host instructions comprise  
VLIW instructions.

30. (Currently amended) The computer readable storage media of claim 28 21,  
wherein the virtual machine comprises an x86 compatible virtual machine.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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